[02885/84]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s)	:	Martin VORBACH et al.
Serial No.	:	10/792,168
Filing Date	:	March 2, 2004
For	:	I/O AND MEMORY BUS SYSTEM FOR DFPS AS WELL AS MODULES HAVING TWO- OR MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURES
Group Art Unit	:	2111
Examiner	:	Gopal C. Ray
Confirmation No.	:	3713

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
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Date Feb 2, 2007 Atty's Reg. # 36,098
Atty's Signature
MICHELLE CARNIAUX
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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE AFTER FINAL REJECTION

SIR:

This paper addresses the Final Office Action dated August 18, 2006. Initially, please amend the above-captioned application without prejudice as follows:

Remarks begin on page 2 of this paper.